In The Claims:

Claim 1. (original) An operation method of a control chip for accelerating a memory access operation, wherein the control chip is coupled to a Central Processing Unit (CPU), the operation method comprising:

receiving from the CPU a first address strobe signal, a request signal, and an address bus signal that refer to a first clock, wherein the request signal comprises a selection phase and a length phase, and the address bus signal comprises an address phase and a byte enable phase;

issuing a second address strobe signal that refers to the first clock when the selection phase indicates either a memory read request signal or a memory write request signal and the address phase indicates an effective memory address;

converting the second address strobe signal that refers to the first clock to a third address strobe signal that refers to a second clock;

issuing an enable signal that refers to the first clock when a specific condition indicative of an invalidate memory cycle is not suggested; and

issuing a memory control signal that refers to the second clock when both the third address strobe signal and the enable signal are enabled.

Claim 2. (original) The operation method of Claim 1, wherein the first address strobe signal is issued when the CPU initializes a memory cycle.

Claim 3. (original) The operation method of Claim 1, wherein the first clock is a CPU clock and the second clock is a memory clock.

Claim 4. (original) The operation method of Claim 1, wherein the selection phase

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is used to define a transmission type of the request signal and the length phase is used to define a memory length that is accessed by the request signal.

Claim 5. (currently amended) The operation method of Claim 1, wherein the address phase is used to define an address of ~~the~~ an memory location and the byte enable phase is used to select a byte data, a word data, a double word data, or a quad word data for the memory access operation.

Claim 6. (original) The operation method of Claim 1, wherein the specific condition indicates that a memory length indicated by the length phase is a specific data type in the length phase and simultaneously all bytes of the byte enable phase are disabled in the byte enable phase.

Claim 7. (original) The operation method of Claim 6, wherein the specific data type is a quad word data format.

Claim 8. (currently amended) The operation method of Claim 1, wherein the control chip comprises a microprocessor interface for receiving the first address strobe signal, the request signal, and the address bus signal to generate the second address strobe signal and the enable signal~~, wherein two of the adjacent second address strobe signals are not continuously issued by the microprocessor interface~~.

Claim 9. (original) The operation method of Claim 1, wherein the control chip comprises a signal conversion circuit for converting the second address strobe signal that refers to the first clock into the third address strobe signal that refers to the second clock.

Claim 10. (original) The operation method of Claim 1, wherein the control chip comprises a memory interface, a control signal referring to the second clock is issued for

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controlling the memory access operation when both the third address strobe signal and the enable signal are enabled..

Claim 11. (currently amended) An operation method of a control chip for accelerating a memory access operation, where the control chip is coupled to a Central Processing Unit (CPU), the operation method comprising:

receiving from the CPU a first address strobe signal, a request signal, and an address bus signal that refer to a CPU clock, wherein the request signal comprises a selection phase and a length phase and the address bus signal comprises an address phase and a byte enable phase;_

issuing a second address strobe signal that refers to the CPU clock when the selection phase indicates either a memory read request signal or a memory write request signal and the address phase indicates an effective memory address;_

issuing an enable signal that refers to the CPU clock when a zero-length signal is not suggested, wherein the zero-length signal indicates that a memory length indicated by the length phase follows a quad word data format and simultaneously all bytes of the byte enable phase are disabled; _

converting the second address strobe signal that refers to the CPU clock to a third address strobe signal that refers to a memory clock; and_

generating a memory control signal that refers to the memory clock when both the third address strobe signal and the enable signal are enabled, wherein the memory control signal is not issued when the enable signal is disabled due to the zero-length signal is suggested.

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Claim 12. (original) The operation method of Claim 11, wherein the request selection phase is used to define a transmission type of the request signal and the length phase is used to define a memory length that is accessed by the request signal.

Claim 13. (currently amended) The operation method of Claim 11, wherein the address phase is used to define an address of ~~the~~ a memory location and the byte enable phase is used to select a byte data, a word data, a double word data, or a quad word data for the memory access operation.

Claim 14. (currently amended) The operation method of Claim 11, wherein the control chip comprises:

a microprocessor interface for receiving the first address strobe signal, the request signal, and the address bus signal to generate the second address strobe signal and the enable signal~~, wherein two of the adjacent second address strobe signals are not continuously issued by the microprocessor interface~~;

a signal conversion circuit for converting the second address strobe signal that refers to the CPU clock into the third address strobe signal that refers to the memory clock; and

a memory interface for issuing a control signal referring to the memory clock and used for controlling the memory access operation when both the third address strobe signal and the enable signal are enabled.

Claim 15. (currently amended) A control chip for accelerating a memory access operation, coupled to a Central Processing Unit (CPU), the control chip comprising:

a processor interface for receiving a first address strobe signal, a request signal,

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and an address bus signal from the CPU that refers to a CPU clock, wherein the request signal comprises a selection phase and a length phase and the address bus signal comprises an address phase and a byte enable phase, wherein when the selection phase indicates either a memory read request signal or a memory write request signal and the address phase indicates an effective address range of the memory, the processor interface issues a second address strobe signal that refers to the CPU clock, wherein the processor interface issues an enable signal that refers to the CPU clock when a specific condition indicative of an invalidate memory cycle is not suggested in the length phase and the byte enable phase;

a signal conversion circuit, coupled to the microprocessor interface for converting the second address strobe signal that refers to the CPU clock to a third address strobe signal that refers to a memory clock; and

a memory controller, coupled to the signal conversion circuit for generating a memory control signal when both the third strobe signal and the enable signal are enabled, wherein the memory control signal is generated by referring to the memory clock.

Claim 16. (original) The control chip of Claim 15, wherein the processor interface comprises a decoding circuit for decoding the first strobe signal, the request signal, and the address bus signal, and output the second strobe signal and the enable signal.

Claim 17. (original) The control chip of Claim 15, wherein the memory interface comprises an arbitration circuit for detecting whether both the third strobe signal and the

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enable signal are enabled or not.

Claim 18. (original) The control chip of Claim 15, wherein the specific condition indicates that a memory length indicated by the length phase is a quad word data format and simultaneously all bytes of the byte enable phase are disabled.

Claim 19. (currently amended) The control chip of Claim 15, wherein two adjacent second address strobe signals are not continuously issued by the microprocessor interface in two continuous cycles of the first clock.

Claim 20. (original) The control chip of Claim 15, wherein the control chip is mounted on a motherboard.

Claim 21. (new) The operation method of Claim 8, wherein two of the adjacent second address strobe signals are not continuously issued by the microprocessor interface in two continuous cycles of the first clock.

Claim 22. (new) The operation method of Claim 14, wherein two of the adjacent second address strobe signals are not continuously issued by the microprocessor interface in two continuous cycles of the first clock.

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